30. The flash memory device according to claim 29, wherein said number can be corrected in accordance with an error check code, that is one.--

REMARKS:

This is in response to the Office Action dated April 18, 2000, which was paper #4 of the present application. Pursuant to this amendment, claims 1-2 and 4-30 are pending in the present application. Reexamination and reconsideration are respectfully requested.

The Office Action states that applicant has not filed the priority document for this application. Applicant submits that the priority document for this application was filed with the U.S. Patent and Trademark Office. Applicant attaches to this amendment a copy of the postcard stamped by the U.S. Patent and Trademark Office indicating receipt of the priority document, a copy of applicant's transmittal letter, and a copy of the first sheet of the priority document.

The Examiner objects to informalities in the drawings. Applicant submits proposed amendments to the drawings, indicated in red on the attached sheets. Should the Examiner approve the proposed changes, applicant will include these changes in replacement formal drawings.

The Examiner objects to claims 1 and 2. Applicant amends claims 1 and 2 to address this rejection.

Claim 19 stands objected to as being an improper claim. The Office Action states that claim 19 is a duplicate of claim 4. Applicant respectfully disagrees. Claim 4 is directed to a flash memory system that may be implemented as distinct components, such as illustrated in FIG. 1 where control unit 8 is shown apart from memory 9. By contrast, claim 19 is directed to the more integrated embodiment illustrated in FIG. 6, where component 9 includes both of a control circuit 11 and a memory cell array 10. As such, the claims are directed to different subject matter and each is proper. Applicant requests withdrawal of this objection.

The Office Action rejects claims 18 and 19 as failing the best mode requirements of section 112. Applicant respectfully submits that the best mode requirement is a requirement for the specification and not for the claims. As such, this is an improper best mode rejection. Nevertheless, applicant has amended claims 18 and 19 to delete the rejected phrase.

The Examiner rejects claims 1, 2 and 5-9 as indefinite. Applicant amends claims 1, 2 and 5-9 to address the Examiner's rejection.

The claims stand rejected as anticipated by U.S. Patent No. 5,504,760 to Harari, et al. Applicant submits that the claims pending in this application distinguish over the Harari patent and that these claims distinguished over the Harari patent independent of any amendments to the claims.

The Harari patent describes a flash memory in which an error correction code (ECC) is used to determine if errors remain in a memory block. For example, if the ECC indicates that errors remain during a write operation, at least one of the memory cells in the block has not been written properly. If such errors exist in the Harari patent's memory, the memory writing operation ***always continues*** until the ECC indicates that no memory cell write errors exist. If the memory block cannot be written to without errors, then the block is marked as erroneous and is not used for storage. The Harari patent's memory never leaves an uncorrected memory bit in a block of memory that is used for active storage.

By contrast, the present application describes a memory in which data are encoded when stored and where the memory will consider a write operation to be complete even if at least one erroneous memory bit (an improperly written memory cell) exists in this block. The erroneous memory bit is accepted in the present application's memory if the encoding scheme is such that it provides the correct value of the erroneous memory. This allows data to be written more rapidly and for less perfect memory blocks to be used for effectively storing data.

Data are stored in the present application's memory as encoded symbols. Parity bits, for example of the type used in Reed-Solomon error correction strategies, are added to a string of data to provide redundancy. This is similar to

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what might have been contemplated by the Harari patent. What is different is what is done with that encoding of the data. In the Harari patent, the error correction code is used only to identify the erroneous bit and attempt to correct it. This is illustrated in column 21, lines 46-49 of the Harari patent that shows the step 639, identification of a correctable error, is always followed by a correction step 640. If an error is not correctable, then the block is marked as unusable.

In accordance with the embodiments described in the application, the error correction code bits that make it possible to identify an error are stored in addition to the memory bits that make up the block of memory encoded by those bits, that is, a complete error symbol is stored. This allows the memory block to include an uncorrectable memory bit error or just to have an uncorrected memory bit. The error correction encoding is used to mathematically correct the erroneous memory cell value during data readout. Consequently, the memory described in the present application allows memory blocks to be used effectively even if those blocks have uncorrectable or uncorrected errors.

Aspects of this embodiment are reflected in different ways in the pending claims. Claim 1 requires that the controlling method determine the completion of proper modification of the data in a group of memory units even though there is a detected error if that error can be corrected:

> "determining the completion of proper modification of said data of said group of memory units provided that an error is detected and said error can be corrected."

The Harari patent does meet this limitation because the Harari patent never considers a write or erase operation "proper" if there remains a detected error in the group of memory cells. As such, claim 1 distinguishes over the art of record and is in condition for allowance.

Claim 2 distinguishes over the Harari patent by reciting:

> "determining [the] completion of proper erasure of said data of said group of memory units provided that the counted number of errors is within a correctable range."

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The Harari patent does meet this limitation because the Harari patent never considers an erase operation "complete" if there remains a detected error in the group of memory cells. As such, claim 2 distinguishes over the art of record and is in condition for allowance.

Applicant notes that the Harari patent also does not count errors. The generation of error correction codes does not normally generate a count of errors; neither does an error check operation. Thus, while errors may be corrected in the Harari patent's memory, there is no count of the number of errors. Applicant notes that the Harari patent does keep count of the number of erase and write cycle a memory experiences, but the patent does not count the number of errors in a block.

Claim 4 distinguishes over the Harari patent by reciting:

> determining the completion of proper data modification of data provided that the number of errors detected by said error detection unit is not greater than a number which can be corrected in accordance with an error check code.

As discussed above, the Harari patent's memory never considers a data modification operation complete is errors remain. Additionally, as discussed above with respect to claim 3, the Harari patent's memory does not count errors within a cluster of memory cells. As such, claim 4 distinguishes over the Harari patent and is in condition for allowance.

The claims remaining in this application all recite similar limitations and so similarly distinguish over the Harari patent and are in condition for allowance. The newly added claims 23-30 recite aspects of counting the number of errors in a memory cell array and make error judgements on the basis of the counted number of errors. Neither of these functions is performed in the Harari patent's memory. As such, new claims 23-30 are similarly in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

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If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number 310-282-2000 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

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By: _____

William H. Wright
Registration No. 36,312
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

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